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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/671,875	09/28/2000	Geoffrey Owen Blandy	AUS9-2000-0587-US1	7126

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EXAMINER	
TSAI, HENRY	
ART UNIT	PAPER NUMBER
2183	4

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Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No.	Applicant(s)	
	09/671,875	BLANDY, GEOFFREY OWEN	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) __ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) ____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *2/1/01* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following

at page 1, all application numbers are missing. Similar problems exist in the other pages such as pages 11 and 12.

Appropriate correction is required.

Claim Objections

2. Claims 5, 7, 8, 11, 20, 21, 24, 33, 34, and 37 are objected to because of the following informalities:

In claim 5, line 3, "is" should read -are- since the steps is plural.

In claim 7, it is not clear what is meant by "creating one or more instruction bundles is performed based on a most common instruction combination first"; and in claim 8, line 3-4, it is not clear what is meant by "and proceeds to less restrictive instruction type placement second" since during creating an instruction bundle, the relationship between the first and the second was not defined previously. Similar problems exist in claims 20, 21, 33 and 34.

In claim 7, the definition of "a most common combination" was not defined previously since how to set up a "common" level is unclear. Similar problems exist in claims 20, and 33.

In claim 8, the definition of "a most restrictive" and "less restrictive" were not defined previously since how to set up a restrictive level is unclear. Similar problems exist in claims 21, and 34.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Hull et al. (USP 5,922,065) (Herein referred as Hull et al.)

Referring to claims 1, 14, and 27, Hull et al. discloses as claimed, a method for creating instruction bundles (comprising slot0, slot1 and slot2, see Fig. 4), comprising:

receiving an instruction group (see Col. 4, lines 1-2) having one or more instructions (comprising the instruction types in the table 20 as shown in Fig. 2); determining a number of each possible type of instruction in the one or more instructions of the instruction group limitations (see Fig. 4, the instructions are grouped into different groups separated by the double lines 42 and 43; and the stop bits (S-bit see Fig. 3), see also Col. 4, lines 43-45, and lines 61-67, each group comprises different execution unit types, such as I-unit, M-unit, and F-unit see Figs. 2 and 4 based on the architectural limitations thereof); and creating one or more instruction bundles (comprising slot0, slot1 and slot2, see Fig. 4) based on the number of each possible type of instruction in the one or more instructions of the instruction group (as set forth above, see Fig. 4, the instructions are grouped into different groups separated by the double lines 42 and 43; and the stop bits (S-bit see Fig. 3), see also Col. 4, lines 43-45, and lines 61-67, each group comprises different execution unit types, such as I-unit, M-unit, and F-unit see Figs. 2 and 4 based on the architectural limitations thereof).

As to claims 2, 15, and 28, Hull et al. also discloses: receiving an instruction group having one or more instructions includes receiving a stream of intermediate instructions

(comprising the instruction types in the table 20 as shown in Fig. 2) organized into instruction groups.

As to claims 3, 16, and 29, Hull et al. also discloses: gathering information about an architecture for use in creating instruction bundles (comprising slot0, slot1 and slot2, see Fig. 4. Note each group comprises different execution unit types, such as I-unit, M-unit, and F-unit see Figs. 2 and 4 based on the architectural limitations thereof).

As to claims 4, 17, and 30, Hull et al. also discloses: the information includes at least one of a number of each type of execution unit available in the architecture and a number of bundles (as set forth, each bundle comprising slot0, slot1 and slot2, see Fig. 4. Note each group comprises different execution unit types, such as I-unit, M-unit, and F-unit see Figs. 2 and 4 based on the architectural limitations thereof) that can be dispatched concurrently by the architecture (see Col. 4, lines 1-2, regarding "a instruction group is a set of statically contiguous instructions that may be executed concurrently").

As to claims 5, 18, and 31, Hull et al. also discloses: the steps of determining a number of each possible type of instruction and creating one or more instruction bundles is performed for each instruction group in the stream of

intermediate instructions (comprising the instruction types in the table 20 as shown in Fig. 2).

As to claims 6, 19, and 32, Hull et al. also discloses the steps of: creating one or more instruction bundles is performed in view of one or more of the following rules: 1) instructions of the same instruction type will preserve there original order (note the above step is inherently disclosed in the Hull et al.'s system since as shown in Fig. 4, such as the bundle in template 0, I-unit in slot2 follows I-unit in slot1); 2) branches will normally appear only in the final bundle of an instruction group (note the above step is inherently disclosed in the Hull et al.'s system since as shown in Fig. 4, such as the bundle in templates 8 and C, B-unit is in slot2, in the final bundle of an instruction group when the stop bit is 1, see Fig. 3); 3) for architectures where a number of M execution units is equal or less than a number of concurrent bundles, MM templates will only be used when there are three or fewer instructions remaining in the group; 4) instructions are taken in order of their flexibility in terms of where that instruction can be placed in the available bundle types; and 5) MBB and BBB templates are avoided when only a single B instruction remains (note the above steps 3) and 4) are inherently disclosed in the Hull et al.'s system, as set forth, each bundle comprising

slot0, slot1 and slot2, see Fig. 4. Note each group comprises different execution unit types, such as M-unit, and B-unit see Figs. 2 and 4 based on the architectural limitations thereof in order to avoid stall for increasing the process performance).

As to claims 7, 20, and 33, Hull et al. also discloses, as best understood: 7. The method of claim 1, wherein creating one or more instruction bundles is performed based on a most common instruction combination first (note each bundle comprises different most common instruction combination using execution unit types, such as I-unit, and M-unit, see Figs. 2 and 4 based on the architectural limitations thereof).

As to claims 8, 21, and 34, Hull et al. also discloses, as best understood: creating one or more instruction bundles is performed based on a most restrictive instruction type placement (such as the bundle with template 0 having M-unit since memory access should be processed first to fetch operands) and proceeds to less restrictive instruction type placement (such as the bundle with template 0 having I-unit since integer operation needs operands to be fetched first) second.

As to claims 9, 22, and 35, Hull et al. also discloses: creating one or more instruction bundles is performed based on a most restrictive instruction type placement (such as the bundle with template 0 having M-unit since memory access should be

processed first to fetch operands) and proceeds to less restrictive instruction type placement (such as the bundle with template 0 having I-unit since integer operation needs operands to be fetched first).

As to claims 10, 23, and 36, Hull et al. also discloses: determining a number of each possible type of instruction in the one or more instructions of the instruction group includes incrementing instruction counters (see Col. 5, lines 15-18, regarding "bundles are ordered from lower to highest memory address. Instructions in bundles with lower memory address are considered to precede instructions in bundles with higher memory address"; see also Col. 5, lines 20-23, regarding the instruction group being ordered (best broadly and reasonably interpreted as "counted") from instruction slot 0 to instruction slot 2 as shown in Fig. 3) based on the number of each possible type of instruction in the one or more instructions, and wherein creating one or more instruction bundles includes decrementing the instruction counters as instructions are added to instruction bundles (see Col. 5, lines 15-18, regarding "bundles are ordered from lower to highest memory address. Instructions in bundles with lower memory address are considered to precede instructions in bundles with higher memory address" as set forth above, see also Col. 5, lines 20-23, regarding the instruction

group being ordered (best broadly and reasonably interpreted as "counted") from instruction slot 0 to instruction slot 2 as shown in Fig. 3).

As to claims 11, 24, and 37, Hull et al. also discloses: the most common instruction combination is where all instructions in the instruction group are of a memory instruction type, integer instruction type or integer arithmetic logic unit type (note each bundle comprises different most common instruction combination using execution unit types, such as I-unit, and M-unit, see Figs. 2 and 4 based on the architectural limitations thereof).

As to claims 12, 25, and 38, Hull et al. also discloses: creating one or more instruction bundles includes ensuring that creating the one or more instruction bundles does not introduce hardware oversubscription (note each bundle comprises different most common instruction combination using execution unit types, such as I-unit, and M-unit, see Figs. 2 and 4 based on the architectural limitations thereof to avoid hardware oversubscription).

As to claims 13, 26, and 39, Hull et al. also discloses: ensuring that creating the one or more instruction bundles does not introduce hardware oversubscription includes forming partial instruction bundles (see Fig. 4, the instruction bundles with

templates 1 and 5 having double lines 42 and 43 used as a separator for different groups, the instruction bundles are best reasonably and broadly interpreted as a partial instruction bundle).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, such as Sharangpani et al'077; Vassiliadis et al.'932; and Garg et al.'499 also disclosing the similar limitations as claimed.

Contact Information

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (703) 308-7600. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (703) 305-9712. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to

the **TC 2100 receptionist whose telephone number is (703) 305-3900.**

7. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into: **the Group at fax number: 703-872-9306.**

This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER
December 23, 2003